imec NEWSLETTER 45

JULY 2006

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News from IMEC's M4 program | TECHNOLOGY REPORT

IMEC's software-defined radio concept **compliant with 3GPP-LTE**

IMEC has demonstrated on the air 3GPP-LTE compliant data transmission, from a first FPGA-based hardware-software prototype of its flexible-air-interface (FLAI) platform. IMEC also demonstrated a software transaction-level model representation of this FLAI platform, as first implementation step towards a 90nm chip tape-out of the FLAI-SDR (software-defined radio) platform beginning next year.

3GPP-LTE-like transmission is demonstrated wirelessly over the air with real-time transmission and non-real-time receiver post processing on IMEC's first prototype of its FLAI platform. The system makes use of novel terminal synchronization and analog front-end non-ideality compensation (crystal frequency offset, IQ imbalance, phase noise) techniques to achieve a high spectral efficiency. IMEC has patented a technique to acquire the carrier frequency offset (CFO) in the presence of IQ imbalance, based on a newly designed preamble. The accuracy of the CFO estimation is very high, achieving a few hundreds Hertz for a typical IQ imbalance.

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News from IMEC's (sub-)32nm research platform

NEWS FLASH

IMEC shows potential of **FUSI for low-power applications** and its extendibility to high performance

Device performance meets ITRS for 45nm

IMEC realized several breakthroughs on Ni-based FUSI making it a manufacturable and reliable process for the 45nm node. Excellent low-power, high-performance specifications were achieved. The process window has been improved and the work function can be modulated in a practical way.

IMEC has demonstrated the potential of fully-silicided (FUSI) gates meeting the 45nm-node ITRS specifications. A ring oscillator using low-power CMOS transistors with Ni-based FUSI gates on HfSiON achieved a record unloaded delay of 17ps at an Ioff of 20pA/µm and VDD of 1.1V. The use of metal gates realized with the FUSI process enabled further gate-length reduction to 7nm for NMOS and 14nm for PMOS over poly-Si/SiON.

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Editorial

The semiconductor industry… is there a more challenging industry in the world? While the industry is working hard to introduce the 45nm technology node into the development stage, we, at IMEC, have focused our programs completely on continued scaling towards 32nm and beyond. Lithography is this time one of the most critical factors. Extreme UV will for sure be needed to accommodate the pitch requirements for sub-32nm CMOS, but it still has a long way to go before it can be inserted into manufacturing. As such, it will be necessary to extend 193nm immersion lithography down to 32nm CMOS. As a result, 193nm immersion litho will be pushed to its limits, including extensive use of double-patterning techniques.

Up to now, industry, research centers and universities managed, in one way or another, to cope with the ever more complex bottlenecks in scaling CMOS. One could doubt if we will be able to continue winning this technological battle. When I look back to the early eighties when IMEC was established and what we have realized in more than 20 years, I'm firmly convinced that we are stronger than ever.

If one would ask me to pick a 3-word battle cry that describes IMEC's approach to assist the semiconductor industry in its quest for ever cheaper, smarter and more energy efficient chips, I would say "EXECUTE, INNOVATE, RESPOND".

Execute. Ideas and models of research teams have to be realized. Today, IMEC is more than ever ready to do this in its state-of-the-art 300mm cleanroom. We just finished the installation of the back-end-of-line equipment, with first full-flow lots being processed. This fully operational FEOL and BEOL 300mm infrastructure, realized thanks to the close partnerships with equipment suppliers and contributions of the core partners and the government of Flanders, certainly is a unique asset for a research centre. The combination with the formerly built 200mm cleanroom allows us to use a flexible technology platform to perform research on and demonstrate new applications such as biosensors, MEMS, GaN devices etc. This is very important for combining and converging the More-Moore and More-than-Moore worlds.

Innovate. More than ever, the semiconductor industry must be innovative. Universities play a crucial role to create innovative ideas and investigate their feasibility together with research centers. I'm glad that IMEC can build on numerous PhDs and on collaboration with an elaborate university network. It guarantees a high-level of long-term and exploratory work to establish a strong base for future work (for example research on new channel materials such as germanium; research on carbon nanotubes). Last year, we had more than 100 active collaborations with universities in Flanders, Europe and the rest of the world, jointly building the future of our (sub-)32nm CMOS platform.

Respond. Research needs to be responsive. It must, in a flexible manner, follow the changing market and industrial needs. A global research platform, such as our (sub-)32nm platform, ideally fits this need. By closely working together and setting up partner meetings on a regular base, information is exchanged continuously, allowing us to quickly anticipate the changing environment. For example, at present, some programs are shifting focus to better deal with the challenges for the 32nm technology node. The advanced-litho program runs hyper-NA immersion, double-patterning immersion and EUV lithography in parallel, the front-end program redirects its attention from FUSI to metal-inserted poly gates (MIPS), and the interconnection program studies now low-k materials with k value lower than 2.5.

I'm looking with confidence and curiosity to the future of the semiconductor industry. Confident, because I strongly believe that our researchers and worldwide partner network will be able to beat even the hardest 'roadblocks' and continue on Moore's road and beyond. If we only keep following our battle cry. Curiosity… well, our history was full of surprises. No doubt, future technology will bring even more interesting surprises…

Luc Van den hove,
Vice President Silicon Process and Device Technology

IMEC demonstrates growth of **AlGaN/GaN high-electron mobility transistor** structures on 150mm silicon

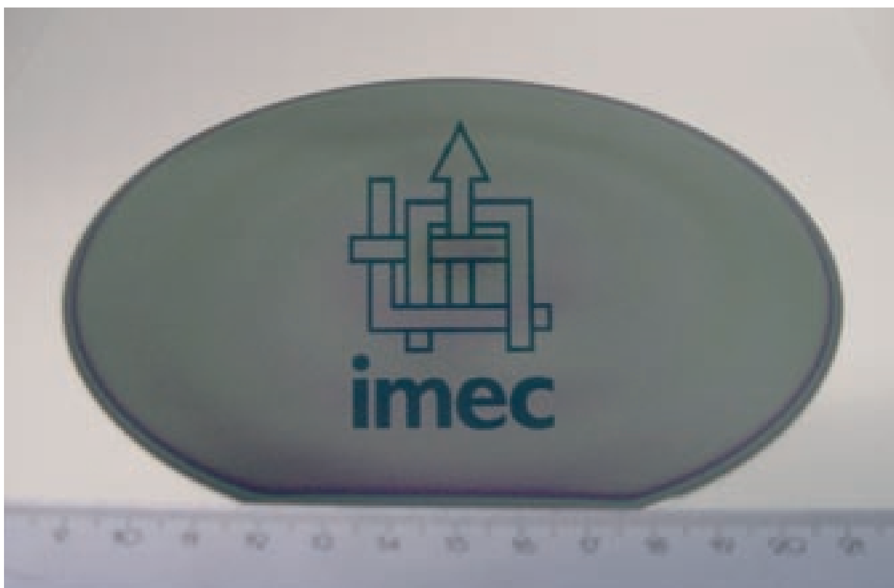
IMEC has demonstrated the growth of low-sheet-resistivity AlGaN/GaN high-electron mobility transistors (HEMTs) heterostructures on 150mm silicon (Si) wafers. The process paves the way to low-cost GaN power devices for high-efficiency/high-power systems beyond the silicon limits. The high-quality AlGaN and GaN layers, leading to the formation of a two-dimensional electron gas, with excellent electrical characteristics, were grown in IMEC's new 150mm metal-organic chemical vapor-phase epitaxy (MOVPE) system.

CCS MOVPE reactor for the growth of III-nitride semiconductors.

Gallium nitride (GaN) has outstanding capabilities for power, high-frequency, low-noise, high-temperature operations, even in harsh environment, extending considerably the application field of solid-state devices. Due to the lack of commercially available GaN substrates, GaN heterostructures are nowadays grown mainly on sapphire and silicon carbide (SiC). Si is a very attractive alternative due to its very low cost compared to sapphire and SiC. Other benefits include the acceptable thermal conductivity of Si (half of that of SiC) and its availability in large quantities and large wafer sizes. The growth of high-quality epitaxial GaN layers is however problematic due to the high lattice mismatch and the large difference in thermal expansion coefficient between Si and GaN.

IMEC has made considerable efforts to develop optimized recipes for growing GaN on Si(111). An AlGaN buffer layer has been successfully introduced to provide compressive stress in the top GaN layer. This, in combination with an in-situ Si_3N_4 passivation layer, results in superb HEMT devices on Si. The procedure recently enabled the growth of HEMT structures on 100mm Si substrates with record sheet resistivity as low as 256±4Ω/square, with an electron mobility in the range of 1500-1800 cm^2/Vs and an electron density ranging from $1.3 \times 10^{13}/cm^2$ to $1.7 \times 10^{13}/cm^2$. Resulting devices, with gate length of 0.2µm, have a maximum current density of 1.1A/mm, a transconductance of 310mS/mm, a maximum oscillation frequency f_{max} of 50GHz and a cut-off frequency f_T of 28GHz.

Moreover, for the first time ever, excellent uniformity results have been obtained on 150mm Si wafers. HEMT structures with a sheet resistivity as low as 272±5Ω/square and a standard deviation as small as 1.9% (edge excluded) have been demonstrated. The high-quality epitaxial AlGaN and GaN layers were grown in IMEC's new 150mm MOVPE Thomas Swan Close-Coupled Showerhead reactor (CCS) system, in the framework of a European Space Agency (ESA) project called Epi-GaN. This second reactor is a very valuable extension of the existing 3x2" vertical CCS system, as it increases both growth capacity and wafer size (up to 150mm). The infrastructural extension allows IMEC to offer laboratories and partner companies involved in the development of GaN device applications a platform for collaboration with IMEC. The obtained results prove the capability of IMEC to grow HEMT epiwafers with excellent quality, good uniformity and high reproducibility. AlGaN/GaN HEMT epiwafers can be grown on sapphire, SiC or Si substrates.



AlGaN/GaN HEMT grown on 150mm silicon wafer.

PRESENTED AT THE 2006 13TH INTERNATIONAL CONFERENCE ON METAL ORGANIC VAPOR PHASE EPITAXY, MIYAZAKI, JAPAN.

Continued from p.1

IMEC's software-defined radio concept **compliant with 3GPP-LTE**

This technique enables successful demodulation of a 64QAM constellation at the receiver and therefore realizes the high data rate promises of the 3GPP LTE air interface in practice. In the demonstration, the received constellation (after channel equalization) is compared to the original one. By activating and deactivating the front-end compensation mechanisms, it is possible to evaluate their effects. The real-time transmit baseband processing is mapped on a VLIW processor and shows the feasibility of implementing a 3GPP-LTE transmitter at low complexity on a software-defined radio.

IMEC also developed a transaction-level model of the complete transmit/receive SDR platform, to support a wide range of standards including 3GPP-LTE, 802.11n, 802.16e and DVB-H. Besides a baseband processor, it includes an ARM processor, a digital front-end core, a forward-error-coding unit and a direct memory access engine for accelerating data transfers. The model allows verifying the complex data movement and synchronization between different blocks of the architecture.

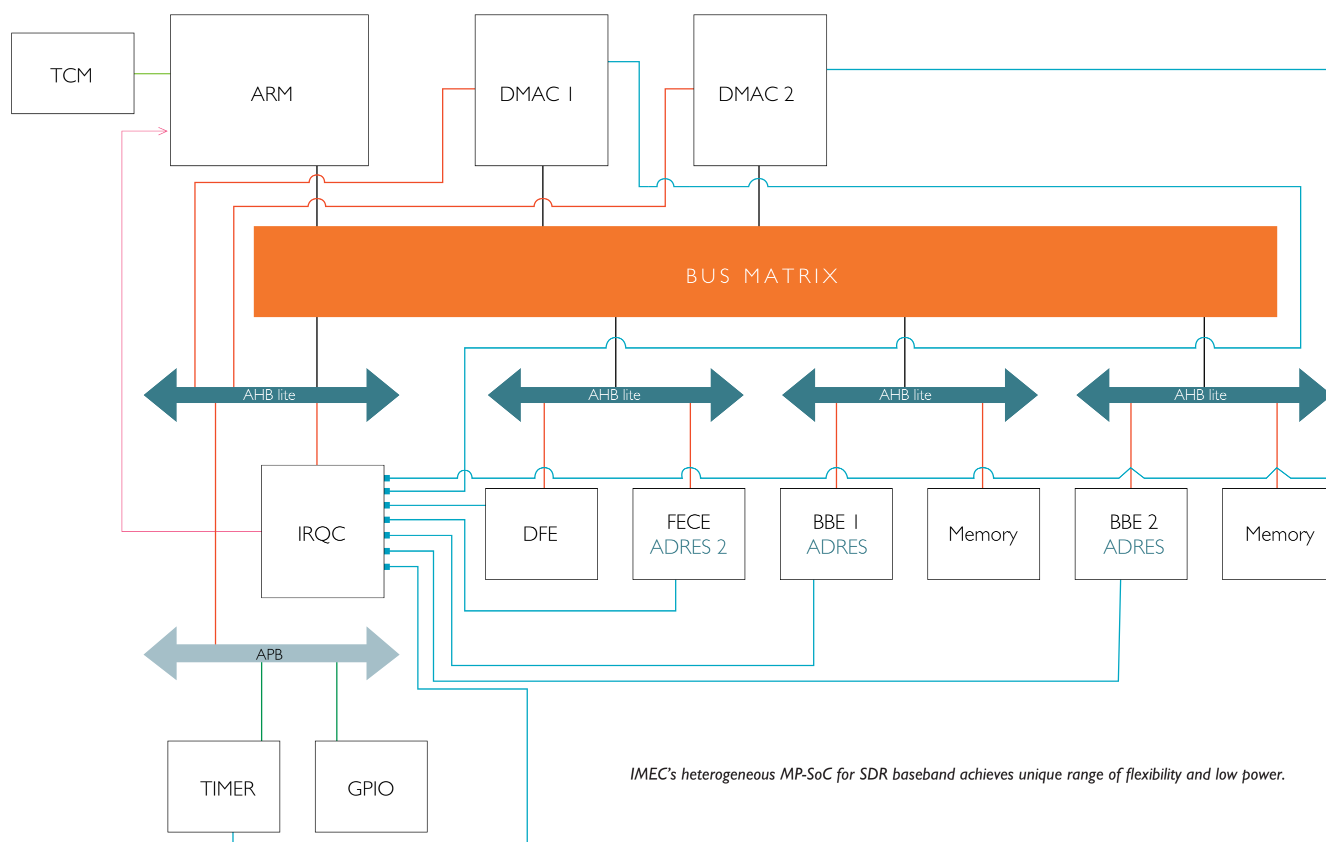
These results were obtained within IMEC's M4 program in which IMEC is building a heterogeneous multi-processor system-on-chip platform enabling flexible implementation of most wireless communication standards at low power. Such a solution is desired by the industry to enable seamless connectivity with first generations of SDR-based mobile terminals and handhelds operating at limited battery energy. The functionality support spans from cellular (CDMA) to next-generation high data rate WLAN-WiMAX-DVB (OFDM-MIMO) standards.

A cross-layer power manager will exploit the scalability and heterogeneity of the platform to enable minimal power for the different operation modes. A white-box design environment allows building scalable retargetable virtual platforms and supports hardware software co-design. It enables efficient development by IMEC partners of their proprietary wireless SDR platforms based on IMEC's FLAI research results.

IMEC's SDR platform comes with an optimized baseband 2D processor based on IMEC's reconfigurable processor, ADRES. A tool suite including a C-compiler is developed together with the ADRES core. Experiments have already demonstrated that the unique ADRES architecture achieves record breaking performance/power of ~0.35mW/MHz by efficiently supporting instruction-level parallelism and data-level parallelism.

A digital front-end ASIP-core (DFE) which detects incoming wireless signals is added to interact with the SDR baseband processor. This enables a first of a kind SDR solution that supports low standby power (~2mW) during idle mode, whilst supporting efficient wake-up of the SDR-baseband processor on incoming multi-mode signals. The DFE functionality together with the high power efficiency of the ADRES core integrated into IMEC's SDR-FLAI solution, will support industry to overcome the major roadblocks for introducing SDR-based baseband in future mass volume mobile terminals.

The SDR solution is completed by an IMEC proprietary SDR radio front-end with building blocks that are designed to offer flexibility in carrier frequency, channel bandwidth, noise performance, etc. without a significant power penalty.



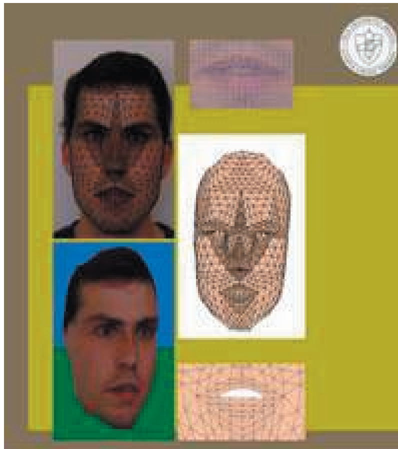
IMEC's heterogeneous MP-SoC for SDR baseband achieves unique range of flexibility and low power.

ETRO develops tools for **audio-visual face expression communication**

ETRO, IMEC's associated lab at the University of Brussels (VUB) has developed tools to integrate both audio and visual components in communication systems. Research currently focuses on the creation of synthetic mouth shapes of a virtual face and emotion recognition in verbal communication. This will be used for a case study with a social robot meant to interact with hospitalized children.

The gestures of a face play an important role in the human-to-human communication. Several recent media applications such as computer games, virtual newsreaders on the internet, and interactive television, make use of a virtual speaking face to support the spoken content. The new trend in the robot industry is to make the robots appear more natural by giving them reactions to observed human emotions and moods. ETRO integrates the audio and visual analysis of speech and gestures to support these applications.

One of ETRO's achievements, in collaboration with the Northwestern University of X'ian (China), is the creation of synthetic mouth shapes of a virtual face corresponding to a spoken sentence. This was done by exploiting the temporal alignment of the visual lip-shape features and the audio-signal characteristics of the smallest audiovisual speech-units, the visemes. The image analysis used in the training phase of this audiovisual system proceeds as follows: the gesture parameter that represents the amount of opening of the mouth and eyes is a combination of the filtered image window details. The deformations of the finer facial expressions are found by exploiting the correspondence between the motion in the image and the motion in the 3D world of a face virtual model and also by imposing mechanical constraints on the face. With this audio-visual analysis scheme a more plausible talking virtual face is achieved than with a (pure audio) phoneme recognizer. The scheme will be further developed as a lip-reading-aid for the training of a correct pronunciation of hearing-impaired children.



Analysis of the motions of a mouth.

Further, a system for the emotion and intent recognition and synthesis in verbal communication with similar integration of speech and image processing is being developed. Machine learning techniques have already been applied to recognize the emotional intent in a voice. By connecting the visual emotion features to the audio characteristics of numerous examples of expressive speech, it is expected that a better separation of the different emotional states can be detected. ETRO is currently expanding the system with the synthesis of syllables of a synthetic voice carrying emotions. For this purpose the features of pitch, rhythm and loudness of expressive speech examples are transferred to a voice. The plan is to attach a synchronized synthesis of the visual counterpart of the expression, based upon the previously mentioned emotion recognition results. This study focuses on following case-studies in both verbal and nonverbal interaction, among them the 'Anty' social robot which is meant to interact with hospitalized children based on their mood. Anty is being developed in collaboration with the department of robotics and multibody mechanics of the University of Brussels (VUB). With the audio-visual emotion system, ETRO is designing a voice for Anty to speak to the children with comfort, compassion, encouragement,… or to sing them a song. A secondary application of the 'prosody-transplantation' part of the system

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  VUB-Department of Electronics and Informatics.
- Audio-Visual Signal Processing, Machine Vision and Digital Speech and Signal processing Groups
  www.etro.vub.ac.be
- '**Facial Analysis and Synthesis**', I. Ravyse, PhD. Thesis, May 2006.
- '**Context dependent viseme models for voice driven animation**', X. Lei, J. Dongmei, I. Ravyse, W. Verhelst, H. Sahli, V. Slavova, Z. Rongchun, 4th EURASIP Conference focused on Video/Image Processing and Multimedia Communications, EC-VIP-MC 2003, pp. 649-654.
- Audio-Visual Systems FWO WOG: **www.avs.vub.ac.be**
- Anty: **http://anty.vub.ac.be/**

Awards

- **Geert Carchon** received the outstanding-poster award for the poster "Integration of 0/1-level packaged RF-MEMS devices on MCM-D at millimeter-wave frequencies," G. J. Carchon, A. Jourdain, O. Vendier, J. Schoebel, and H. A. C. Tilmans, presented at Electronic Components and Technology Conference, Orlando, FL, pp. 1664-1669, May 31-June 3, 2005.
- **Els Parton** received a best-paper award for the paper "Innovative vibrationssensoren," E. Parton, T. Sterken and P. Fiorini, published in E&E Kompendium 2005/2006.
- **Ben Kaczer** received the IRPS outstanding-paper award for the paper "Disorder-controlled-kinetics model for negative bias temperature instability and its experimental verification," B. Kaczer, V. Arkhipov, R. Degraeve, N. Collaert, G. Groeseneken, and M. Goodwin at the International Reliability Physics Symposium 2005, Proceedings p. 381-387.
- **Pierluigi Nuzzo** won the DAC/ISSCC 2006 student design contest with "A 10.6mW/0.8pJ Power-Scalable 1 GS/s 4b ADC in 0.18µm CMOS with 5.8GHz ERBW," P. Nuzzo, F. De Bernardinis, P. Terreni, B. Gyselinckx, L. Van der Perre and G. Van der Plas.
- **Zhe Ma** received the Chinese national award for overseas students of the year 2005.

Backside-thinning of **APS image sensors** increases its sensitivity

In the framework of an ESA project, IMEC together with Cypress Semiconductor Belgium bvba (FillFactory) and Galileo Avionica, developed backside-thinned active-pixel image sensors (APS) of only 35μm thickness. The advantage of these image sensors is that they are CMOS-based and therefore can be integrated with logic circuits to add intelligence to the system. The newly developed thinning procedure allows backside-illumination of the image sensors, increasing their sensitivity. A possible application is earth observation from space.

With the development of CCD image sensors (charge-coupled device), the era of digital cameras and videos started. CCDs are also used in space, for example to observe planets or to perform inspection tasks.

APS image sensors (active-pixel sensor) are a CMOS-based alternative for these CCD sensors. Although less mature, the APS solution is more cost effective and allows to be integrated with logic circuits. The latter is extremely interesting for adding intelligence to the system (for example image compression). For this reason, ESA is very much interested in high-quality APS image sensors.

Today, the sensitivity of APS image sensors is lower than its CCD counterparts. One possible solution to improve its sensitivity is backside-illumination of the sensors. In this case, there are no obstructions for the light particles as there are at the front side (for example metal and oxide layers). Backside-illumination however implies thinning of the sensor substrate, a very difficult procedure. Backside-illumination (and -thinning) has been proven successful for CCD image sensors, but for APS image sensors less expertise is available, especially in Europe.

Thinned 200mm silicon wafer.

35μm-backside-thinned APS image sensor on a readout chip, wirebonded to a test board.

In 2003, IMEC, Cypress Semiconductor Belgium bvba (FillFactory) and Galileo Avionica started the development of backside-thinned APS image sensors within the ESA-funded project "Hybrid APS". Today, in the final stage of the project, a lot of progress has been made. For example, in the field of wafer-thinning, IMEC has worked out a process flow that allows thinning of APS substrates to an ideal thickness of 35μm.

The process flow starts with applying the APS wafer upside down to a carrier substrate. Subsequently, the APS wafer backside is thinned. One of the issues with this process step is the creation of impurities and crystal defects. This is solved by etching, followed by an effective surface treatment (ion implantation and laser annealing). An anti-reflection layer further improves light penetration towards the APS image sensors. Finally, the carrier substrate is removed and electrical connections are realized. For this final step, a second carrier substrate is attached to the thinned backside to give support during the interconnection step.

Together with other results on the design (Cypress Semiconductor Belgium bvba (FillFactory)), thinning and interconnection (IMEC) and quality testing (Galileo Avionica) of APS image sensors, this will in the future allow ESA to send high-quality APS image sensors with built-in intelligence into space. They can be used for earth-observation applications such as the detection of forest fires and desertification, monitoring of crops etc.

SmartHEALTH: smart integrated biodiagnostic systems for healthcare

The IST project SmartHEALTH develops smart diagnostic technologies to be fully integrated into healthcare systems. The prototype systems will provide new solutions for cancer monitoring.

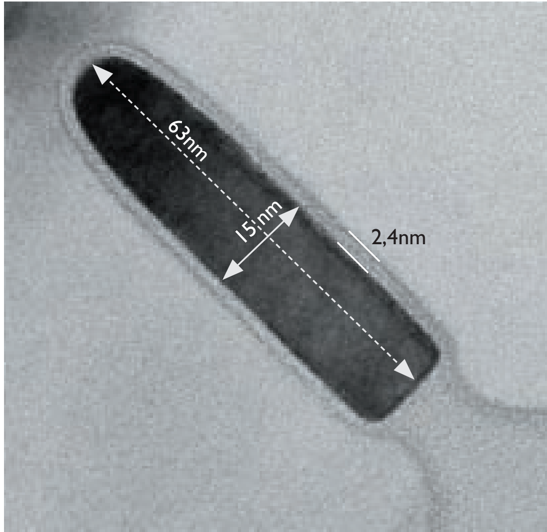
Twenty-eight European partners, including IMEC, collaborate in SmartHEALTH (December 2005 – November 2009) to develop highly intelligent diagnostic technologies that are fully integrated into healthcare systems, optimizing their impact in management and work practice. Driven by key targeted applications in cancer diagnostics (breast, cervical and colorectal), the project will deliver prototype systems with the aim of moving instrumentation from the laboratory, through to portable devices localized at the "point of care".

IMEC's contribution in the project is to develop a fully integrated point-of-care biosensor system based on IMEC's transmission plasmon biosensor technology. This technology should allow to screen several biomarkers in one droop of blood without the need for any additional pretreatment steps or a specialist laboratory. Quantitative results are obtained within a few minutes.

The total cost of the project is 21 million euro, of which 12.3 million euro is received as funding of the European Commission.

More info: www.smarthealthip.com

PullNano: from the 32nm node down to the limits



FinFET, a possible successor of current planar transistors.

The PullNano project was recently launched as a successor of the nanoCMOS project that started in 2004. Over the next two-and-a-half years, the 35 project partners will continue the search for future technology nodes, focusing on the 32nm and 22nm node.

The new EU-funded project PullNano (June 2006 – December 2008) was announced during a two-day training event at the premises of IMEC. The project will continue along the same route as nanoCMOS, pushing further CMOS limits towards 32nm and 22nm technologies. The PullNano project includes 35 partners from 12 countries and is set to receive 25 million euros.

Both projects, NanoCMOS and its successor PullNano aim at pushing the limits of semiconductor performance and density, keeping Europe at the forefront of nanoelectronics. The PullNano project covers exploratory research, characterization, modeling and advanced simulation. demonstration of feasibility of concepts, process-modules integration, definition of specifications of advanced new equipment (of which the assessment will be also performed in the EU funded SEA-NET project), demonstration of feasibility of a 32nm CMOS logic technology and exploratory action towards the 32nm node.

The aim of the project is to work and collaborate around these goals with the main European and international IC manufacturers of the project, the most advanced European research institutes in the field, a large number of European academic teams and finally SME's working in innovative equipment area and modeling and simulation techniques.

ATHLET: Advanced thin-film technologies for cost-effective photovoltaics

Along with 23 other partners from 11 European countries, IMEC participates in the ATHLET project which aims at providing the scientific and technological basis for industrial mass production of cost-effective, highly efficient, environmentally sound, large-area thin-film solar cells and modules.

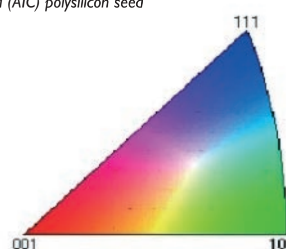
Cost reduction is the central challenge of photovoltaics today. It can be achieved by decreasing the amount of ultra-pure crystalline silicon that is used. The mainstream approach is to adapt the present bulk-silicon technology to realize solar cells on very thin silicon wafers, thinner than 200µm. An alternative approach consists in switching to a thin-film technology, where a very thin layer of a few µm thick is deposited on a low-cost substrate.

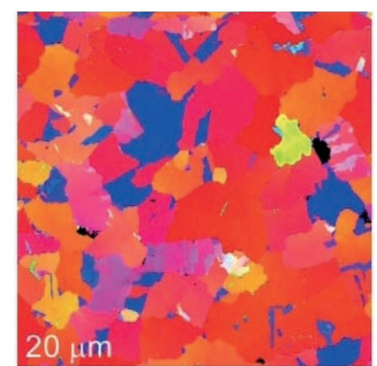
Within the ATHLET project, the partners assess the most promising material and device options for thin-film technologies. The project focuses on cadmium-free cells and modules with the overall goal of providing the scientific and technological basis for industrial mass production of cost-effective, highly efficient, environmentally sound, large-area thin-film solar cells and modules.

IMEC's role within ATHLET is to develop efficient thin-film polycrystalline silicon solar cells. Polycrystalline silicon (with grains size between 1 and 100µm, and a total thickness of less than 5µm) is a relatively new material for thin-film photovoltaics. The technology is less mature than the amorphous and microcrystalline technologies. However, the material has potential for higher efficiencies, and fast progress in this field has been achieved over the last few years. Within ATHLET, IMEC is developing adapted techniques for the formation of large-grained seed layers on low-cost substrates and for epitaxial growth on these seed layers. Whereas the best results so far have been obtained on ceramic substrates, the process will be applied to high-temperature glass, which will enable structures with less shadow and resistive losses. For optimal performance, an efficient light-confinement scheme will be developed for this kind of solar cells.

More info: www.hmi.de/projects/athlet

Orientation Imaging Microscopy (OIM) map of an aluminum-induced crystallized (AIC) polysilicon seed layer on a ceramic substrate.





NEWS FLASH

IMEC annual accounts confirm steady growth

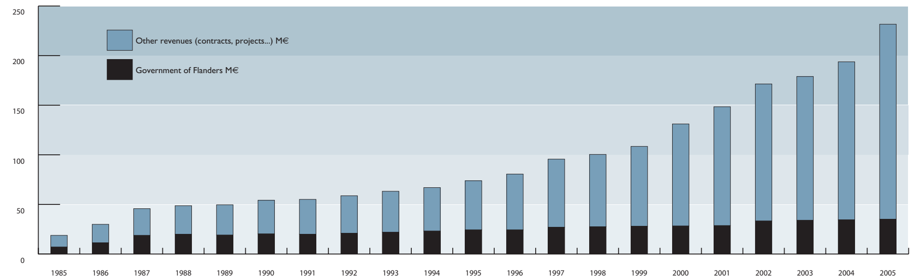
During its General Assembly on April 26, IMEC confirmed a sustained annual increase in revenues since its foundation in 1984. IMEC's performance criteria have increased year over year, a plus in a year when the frame agreement with the government of Flanders will be renewed. The Flemish government accounted for about 18% of the financing for IMEC's research activities in 2005.

In 2005, IMEC's revenue from contract research went up to 157 million euro, bringing the cape of 200 million euros of total revenue in sight. The 197 million euro total revenue represents a firm 23% increase as compared to 2004. The rise primarily results from an increase in revenue from contract research with the international industry. For one of its core activities, research on IC process technologies for the (sub-)32nm generation, IMEC collaborates with eight of the top-ten IC manufacturers and foundries in the world. IMEC receives an annual grant from the government of Flanders amounting to 35 million euro. This grant is indispensable in sustaining IMEC's long-term research.

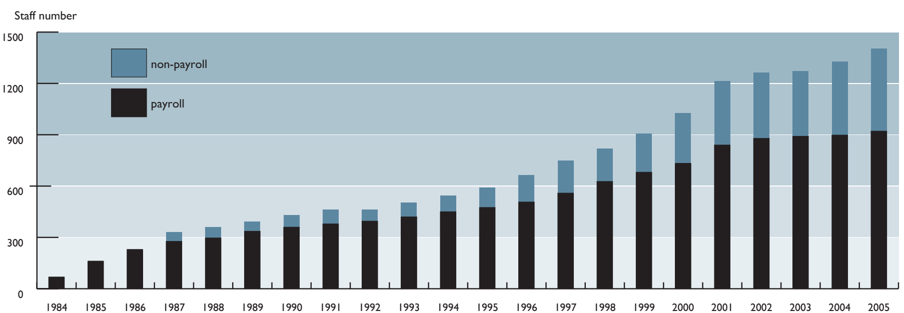
The revenues from contract research were generated through collaboration with local industry (22%) as well as with international industry (68%), through projects of the European Commission (8%) and the European Space Agency (2%). In 2005, more than 550 partners worked with IMEC through a bilateral collaboration, while more than 600 were involved in European projects where IMEC acts as a partner. Additionally, IMEC collaborated with 139 Flemish partners. The quality of IMEC's research was presented in the 1521 scientific papers and conference contributions that IMEC published, often achieved in collaboration with Flemish universities.

* *IMEC's total revenue consists of revenue from contract research, a grant from the government of Flanders and miscellaneous income.*

Evolution of IMEC's annual revenue



Evolution of IMEC's staff number



Microelectronics Training Center: program

IMEC's Microelectronics Training Center (MTC) offers a wide range of courses to a varied and worldwide target audience. In the coming months, IMEC's training program includes the following courses:

- **Basics of biology for engineers**
  October 2-3, 2006, IMEC

  The objective of this course is to introduce basic concepts in the field of biology and biochemistry to laymen in the field. These concepts will allow to grasp the importance of these issues for the field of biotechnology. Formerly of importance to exact science and pharmaceutical industry, but penetrating more and more into other key sectors such as food manufacturing and food quality control.

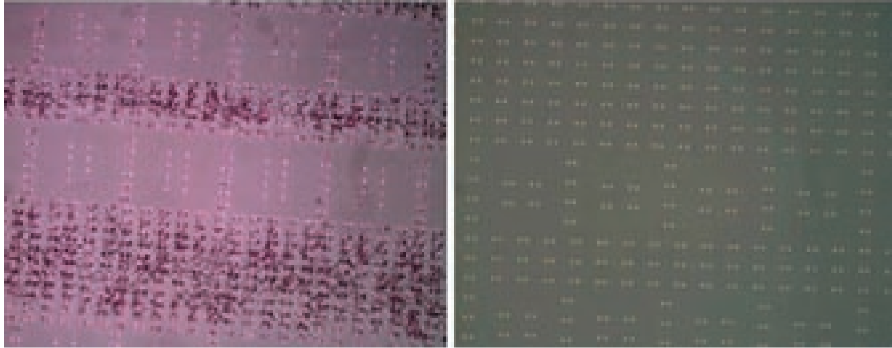
- **Biosensor Technology for scientists and engineers**
  October 4-6, 2006, IMEC

  This introductory course on biosensors is meant to get the interested parties informed on what biosensors are, how they are made, where they are already used and what their future applications are. We want to bridge the gap between wet and dry sciences/engineering to ensure a more fruitful path to commercially successful biosensors and molecular diagnostics.

More info: www.imec.be/mtc or Bart.DeMey@imec.be

First stacking of ultra-thin die with a high-density of through-silicon interconnects.

IMEC reports considerable progress in the development of its 3D-stacked integrated circuits (3D-SIC) technology that uses so-called Cu nails to realize Si-through connections. Results have been obtained for the three key-enabling technologies, namely through-wafer via processing, wafer thinning and Cu-to-Cu thermo-compression technologies.



Optical images of the backside of a wafer with through-wafer vias after thinning down to 17µm by backgrinding and polishing.
(Left) Picture taken after Si-CMP: Cu vias are opened. In the denser via areas, Cu smearing is observed.
(Right) Picture taken after rework with a non-selective slurry: all residues are removed.

The extreme miniaturization of electronic systems requires innovative interconnection and packaging technologies that overcome the limitations imposed by 2D planar architectures. Among the various approaches, drawn up by IMEC in its roadmap for 3D interconnect technologies, the 3D-SIC technology enables the highest interconnect density. IMEC is developing an innovative 3D-SIC approach, by introducing a small Si-via and Cu plug, called 'Cu nail'. This Cu nail is processed between the front-end-of-line and back-end-of-line process steps. It therefore differs from other approaches that introduce the through-vias after finalizing the IC process. The success of this approach depends on three key-enabling technologies: through-wafer via processing, Cu-to-Cu thermo-compression and wafer-thinning technologies.

3D-SIC vias with aspect ratio up to 10

IMEC, in close collaboration with Lam Research, has developed a process to etch deep Si vias into Si wafers using a deep-Si etch chamber. The process of record is resist based and yields a via depth of 48µm for a via diameter of 5µm. Scalloping has been strongly reduced after etch resulting in a rough, rather than a scalloped via sidewall. An alternative process with an aspect ratio of 5 is also available and has been used to integrate first stacks with high-density 3D interconnects.

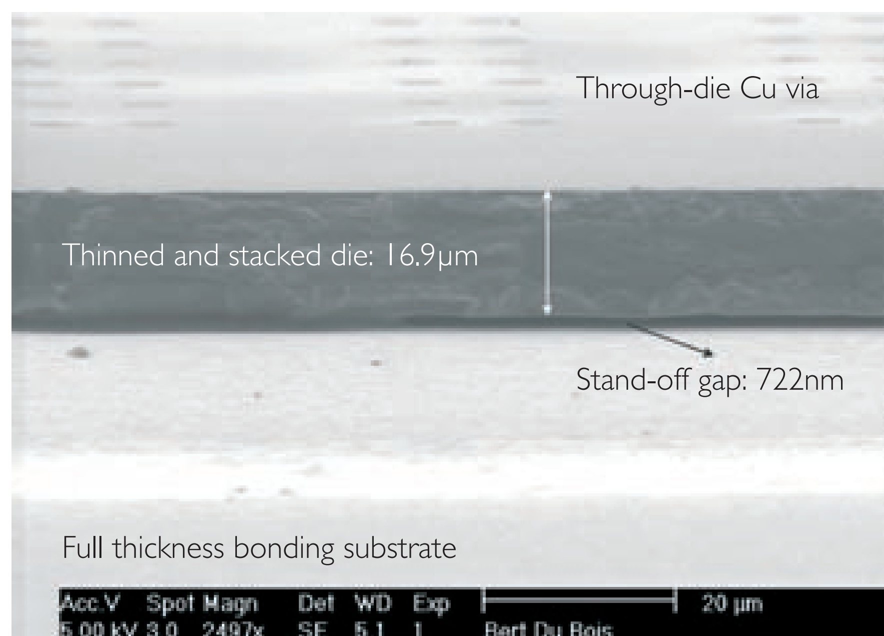
Extreme wafer thinning down to 17µm thickness

Another challenge is related to the thinning of Si down to thicknesses as low as 20µm and to its impact on the device performance. For the first time, IMEC has opened through-wafer Cu vias with a diameter of 5µm and an average pitch of 20µm by extreme wafer thinning. Wafers were first glued to a Si carrier wafer. Next, they were backgrinded to a thickness of 25-28µm (carrier exclusive). The backgrinding process stopped at approximately 7µm above the Cu-vias. In a subsequent Si chemical mechanical polishing (CMP) step, 7-8µm Si were removed, further thinning the wafer down to a thickness of 17µm (carrier exclusive). This CMP step effectively opened the vias and exposed the Cu in the vias. After Si-CMP, smearing of the Cu from the vias was observed, resulting in residues in the most dense via areas. The Cu residues were successfully removed in a short polish step using a non-selective slurry.

First yielding Cu-to-Cu bonding process

One of the main challenges is the development of a mechanically and electrically reliable Cu-to-Cu bonding process. This includes the choice of the dielectric bonding layer, the determination of an optimal bond layer thickness, avoiding Cu oxidation during handling and bonding and an optimization of the bond strengths. IMEC has characterized the Cu-to-Cu thermo-compression bonding process by bonding via-patterned dies to blanket Cu substrates in a flip-chip mode. The quality of the bond was assessed by measuring the force required to shear the patterned die from the blanket substrate when applying a lateral load. This allowed studying the impact of the bonding force, the bonding temperature and the Cu surface preparation on the Cu-Cu bond strength. For dies treated with HCl prior to bonding at a temperature of 350°C, it was found that the bond strength increases with bonding load and saturates when the load exceeds 30kg/die corresponding to ~60MPa per unit area of Cu in the vias. Bond shear strengths consistently larger than 20MPa were obtained when bonding at a temperature of 300°C or higher. Above this temperature, bond strength increases with bonding temperature. Below a bonding temperature of 250°C, the shear strength is low, independent of the bonding temperature. Finally, it was found that samples treated in a dilute citric acid solution prior to bonding, consistently yielded stronger bonds than samples dipped in HCl prior to bonding.

Scanning-electron-microscopy (SEM) pictures of thinned die bonded to a blanket Cu substrate by thermo-compression bonding.



Continued from p.1

IMEC shows potential of **FUSI for low-power applications** and its extendibility to high performance

In addition, IMEC demonstrated that metal gate on HfSiON devices can outperform optimized conventional Poly-Si/SiON 65nm devices by up to 25%.

By using a novel sacrificial SiGe cap at gate level, the process window, manufacturability and reliability have been improved. In a conventional flow, poly-Si and spacer heights are not well controlled before FUSI due to non-uniformity in the CMP process and the need for over-etch at oxide etch-back. The SiGe cap is deposited on the poly-Si film to absorb the process variability resulting in an opening of the process window from ~5°C to ~20°C, meeting manufacturing requirements. In addition, a Vt control with σ~19mV for NMOS and σ~21mV for PMOS has been achieved, including wafer to wafer variation. For a 10 years lifetime, operating voltages of up to 1V were extrapolated for NMOS and up to 1.2V for PMOS devices with controlled NiSi and $Ni_{31}Si_{12}$ or Ni_2Si FUSI gates making it a reliable process.

Up to now, modulating the work function covering low-Vt to high-Vt in Ni-FUSI devices was a challenging task. IMEC developed a practical method to incorporate Ytterbium (Yb) into the gate which enables modulation of the Vt for NFETs. The Yb is pre-doped into poly-Si through ion implementation. The Vt of PFETs is reduced using a Pt alloy into Ni_2Si FUSI and by applying a strained $Si_{0.8}Ge_{0.2}$ channel. Vt's down to 0.25V for NFET (NiSi:Yb) and PFET (Ni_2Si:Pt + SiGe channel) were achieved on SiON without degradation of the dielectric integrity and long channel mobility.

To eliminate the gate depletion effect and enhance transistor performance, metal gates are being introduced as a replacement of conventional poly-Si gates. Ni-based FUSI has received a growing attention for sub-45nm CMOS applications since it eliminates poly depletion, it is compatible with high-k dielectrics, it is a known material in industry and can be integrated in a conventional CMOS flow. The achieved results make FUSI a potential candidate for both low-power and high-performance applications for the 45nm node.

Current research at IMEC focuses on the implementation of strain and on SiON. The extendibility towards 32nm node dimensions is also under evaluation.

PRESENTED AT THE 2006 SYMPOSIUM ON VLSI CIRCUITS

NEWS FLASH

IMEC's 300mm facility delivers first **full-flow silicon lots**

One year after installation of the full front-end-of-line, IMEC's 300mm research facility hits another milestone with the installation of the back-end-of-line tools. First full-flow silicon lots are scheduled to come out beginning of July.

As announced in the newsletter of July 2005, the installation of back-end-of-line (BEOL) tools started in the second half of 2005. The contact and single damascene metal module were developed in the first half of 2006. The first transistor lot finalized with metal1 is expected to come out early July 2006.

The Planar poly/SiON POR (process-of-record) route is selected for the single-level-metal (SLM) pathfinder lot. After NiSi cladding, the wafers continue to pre-metal dielectric deposition. TEOS/Ozone oxide is used for gap filling. The lithography for both the contact and metal1 level is performed on the ASML/1250i immersion scanner. Target dimensions are 90nm for both contact and metal1. Cu is used for both contact fill and interconnect metallization. A PECVD SiOC low-k dielectric with k=3.0 is used as IMD layer with thin SiCN/SiCO dielectric barriers. Metallisation consists of enhanced resputtered PVD TaN/Ta barriers and Cu seed, followed by a 3 component Cu electroplating step and subsequent low down force Cu CMP. The next phase in the 300mm process setup is the development of the dual damascene Cu/low-k module. This will extend the BEOL process capability to metal-3 processing, allowing the realization of small circuits.

In parallel, the 300mm BEOL tool set for developing the interconnect technology for the 32nm node has reached the process acceptance level. Key features of the tool set include PECVD SiOC low-k dielectrics with $k \leq 2.5$, advanced thin dielectric barriers with $k \leq 4.0$, UV cure treatment to enhance low-k film properties, advanced dielectric and metal hardmask etch chambers with integrated wet clean, enhanced resputtered PVD TaN/Ta and ALD TaN metallic barriers, enhanced thin PVD Cu seed, electroplating with thin seed and direct plating capabilities, low down force Cu and barrier CMP. Interconnect R&D for the 32nm node has commenced on 300mm and first results are expected early Q4 2006.

NEWS FLASH

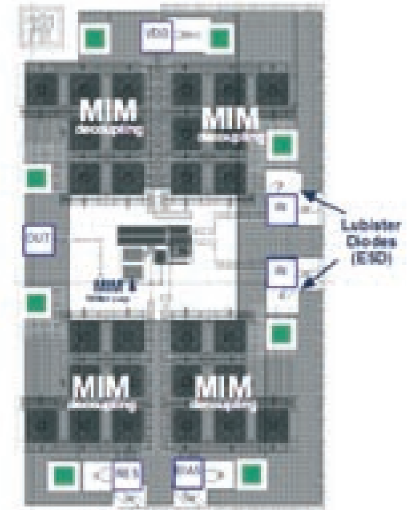
IMEC's (sub-)45nm RF-CMOS program delivers **first functional analog/RF benchmark circuits**

IMEC demonstrated functional amplifiers and oscillators from the first test chip of the (sub-)45nm analog/RF-CMOS program. With these results, the program is on track to perform an early assessment of the analog/RF capabilities of next-generation CMOS nodes.

CMOS scaling is the engine of the continuous improvement of digital applications. It has also been demonstrated that CMOS offers great potential for very high speed or very low power wireless and wireline applications. This potential, together with the high levels of integration that are typical for CMOS technology, and the cost per square mm, allows RF CMOS to compete with SiGe(C) bipolar, BiCMOS and III-V (GaAs, InP) as the technology of choice for new communication demands in volume production. Therefore, it can become a main contributor to the ubiquitous-communication society. The international effort through the ITRS presented a roadmap on the best estimates of introduction time, at the production level, of successive generations of leading technology nodes as well as the R&D needs.

For the 45nm node and below, it will become necessary to introduce revolutionary changes in the materials, process modules and device architectures. Therefore, there is now no worldwide consensus on the variety of device architectures, process modules and new materials. On the other hand, it is important to assess in an early stage the potential of the different options for their analog/RF CMOS performance, in order to establish a long-term analog/RF technology development strategy. In order to maintain a competitive position in the analog/RF domain, significant efforts are needed for a timely exploration and exploitation of the analog/RF applications that will become available in future CMOS technology.

IMEC's (sub-)45nm RF-CMOS program started with an in-depth comparison of analog and RF performance of different device architectures and gate-stack options. Modeling capability was built for planar bulk and FinFET transistors and related passive components. A design environment was created for the design of test structures and benchmark sub-circuits in the frequency range of 5 to 110GHz. From a first reticle, initial demonstrator circuits were already realized such as a FinFET-based Miller-compensated operational transconductance amplifier (OTA) and tunable RF oscillators for ultra-wideband applications. The OTA achieved a gain of 40dB in 2 stages. The tunable oscillator achieved a tuning range of 1-8.5GHz. A new test chip was taped out in January 2006, with a wide variety of low-noise amplifiers, voltage-controlled oscillators, wideband amplifiers etc. for various frequency ranges from a few hundred Megahertz till 110GHz.



FinFET-based Miller compensated OTA with 40dB gain.

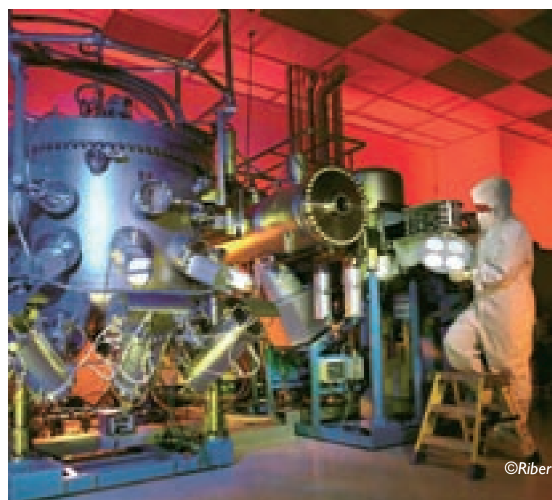
IMEC and Riber collaborate on Ge and III-V devices for the sub-22nm node

Riber, a world-leading supplier of molecular beam epitaxy (MBE) products and services to the compound semiconductor community, joins IMEC's industrial affiliation program (IIAP) on Germanium (Ge) and III-V devices for CMOS beyond the 22nm node. The availability of a unique MBE cluster at IMEC will enable IMEC and its partners to create fundamental know-how on Ge and III-V processing and to develop the core technology ingredients. The program aims to demonstrate that the introduction of Ge and III-V materials allows for CMOS scaling beyond 22nm. Moreover, this collaboration will form the base for a possible extension of the IIAP on Ge and III-V devices beyond mere CMOS into the area of photonic applications.

Research will be performed on Riber's ultra-high vacuum MBE cluster system for 200mm. It includes a III-V compound semiconductor growth chamber and a metal/oxide deposition chamber which will be installed in IMEC's cleanroom. The unique cluster will allow both deposition of compound semiconductor layers on GeOI or other Ge substrates and deposition of high-k dielectrics and metal gates on Ge and on III-V materials. This is considered as a potential enabling technology to make aggressively scaled devices in CMOS beyond 22nm.

The semiconductor industry has cited Ge as a potential replacement for planar silicon, since silicon is unlikely to accommodate the rigorous scaling requirements of sub-22nm geometries. The attractive properties of Ge, such as higher mobility resulting in lower intrinsic gate delay make it an excellent candidate for high-performance CMOS devices, allowing companies to leverage their existing silicon manufacturing infrastructure.

Last year, IMEC has already successfully demonstrated the feasibility of sub-micron PMOS devices on GeOI substrates. To solve the problems that occur with processing Ge NMOS transistors, III-V NMOS devices on the same Ge substrates are targeted. The process will be based on silicon wafers enabling manufacturing in a standard silicon process line using advanced CMOS-compatible equipment. One of the most demanding challenges is to improve the gate stack for MOS devices on Ge as well as on III-V compounds. The Riber MBE cluster will play a crucial role in this development.



Multi-chamber MBE system for large diameter wafers.

The Ge and III-V devices program is part of IMEC's (sub-)32nm CMOS research platform which is being executed with IMEC's core partners Infineon, Intel, Matsushita/Panasonic, Philips, Samsung, ST Microelectronics, Texas Instruments and TSMC, all world leading IDM and/or foundry companies.

NEWS FLASH

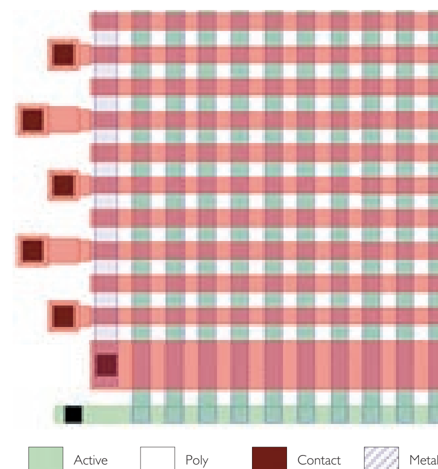
Advanced lithography program extended towards **double-patterning techniques**

Aggressive Flash roadmap redirects lithography roadmap

IMEC's program on advanced lithography, gathering more than 30 tool suppliers, semiconductor manufacturers, material suppliers and mask shops, has shown numerous breakthrough results on 193nm immersion lithography: reduction of patterned defectivity, improvement of CD uniformity and overlay performance. Cornerstone in this research is ASML's TWINSCAN^{TM} XT:1250Di immersion tool.

Today, focus of the program is shifting towards hyper-NA immersion lithography and EUV lithography. Both ASML's XT:1700i hyper-NA tool and full-field EUV scanner will be installed this summer.

However, a lot of research is required before EUV will be ready for manufacturing and hyper-NA immersion lithography will not be sufficient to meet the stringent scaling roadmap of Flash. Therefore, IMEC extends its immersion lithography research program with double-patterning techniques. The double patterning research will be strongly linked with IMEC's advanced-memory program which will focus more on cell scaling. Double-patterning research topics include layout-split methodology and exploration of alternative patterning steps to improve double-patterning cost of ownership. Existing research in the Flash program are the study of new cell concepts (nitride concept), implementation of high-k materials, reliability and characterization. The Flash cell will be used as demonstrator in IMEC's core programs on (sub-)32nm CMOS.



NAND Flash cell layout.

Events

• 21st **European Photovoltaic Solar Energy** Conference & Exhibition

September 4-8, 2006, Dresden, Germany

The ‘who is who’ of the PV solar branch will meet at Dresden to discuss the latest developments in industry and science. Dresden will provide an excellent platform for dialogue and information exchange. This event will contribute to bringing market-oriented and sustainable responses to the challenges of the PV solar energy markets across the world. The conference will be accompanied by workshops and fora. Jef Poortmans, Program Director Photovoltaics IMEC, will be chairman of the EU PV solar energy conference.

More info: www.photovoltaic-conference.com

• **UCPSS 2006** – International Symposium on Ultra-Clean Processing of Semiconductor Surfaces

September 17-20, Antwerp, Belgium

In September 2006, IMEC organizes the eight edition of the UCPSS 2006 Symposium, a biannual event. It is the purpose of the symposium to increase the level of understanding on ultra-clean processing technology in all steps of the IC production. The conference consists of invited presentations as well as selected contributing presentations and posters.

More info: www.ucpss.org

• 3rd International **Symposium on Immersion Lithography**

October 2-5, Kyoto, Japan

This symposium, organized by Selete and SEMATECH in cooperation with IMEC, will continue to guide semiconductor manufacturers and suppliers on progress in 193nm immersion lithography, and to build consensus of emerging critical issues.

More info: www.sematech.org/meetings

• IMEC **Executive Seminar**

November 13, 2006, Hotel New Otani, Tokyo, Japan

IMEC is organizing the seventh edition of it’s Executive Seminar in Tokyo, Japan, at which it will present its latest research results and its industrial cooperation strategy.

The seminar is directed to Executives and Technical Managers and Directors from Japanese semiconductor companies. They will learn more about the significant benefits of collaborating with IMEC. Collaborating with independent research centers such as IMEC offers an effective way of coping with the increasing complexity of advanced ICT systems.

For IMEC, the organization of the seminar is part of its initiative to expand its partnerships to Japan.

More info: www.imec.be/kiosk

• IMEC **ARRM06** > see page 16

October 22-24, 2006, Leuven, Belgium

INDUSTRY LINK

Bekaert and Alcatel join Holst Centre research programs

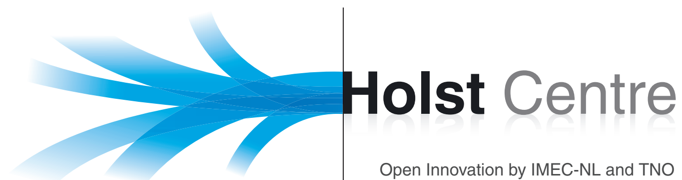
Bekaert has signed a collaboration agreement to join both the Holst Centre's program lines on wireless autonomous transducer systems and system-in-foil products and production. Also Alcatel has joined the Holst Centre research program on wireless autonomous transducer solutions, more specifically as a "Fellow Traveler" for a two-year period.

Bekaert, a world leader in advanced metal transformation and advanced materials and coatings, signed a collaboration agreement with the Dutch R&D institute. Bekaert will join both the Holst Centre's program lines on wireless autonomous transducer systems and system-in-foil products and production. By joining both research programs, Bekaert wants to further reinforce its technological competence and to expand its activities in large area coating of functional layers on flexible substrates. The new technologies and innovations will be proven by groundbreaking demonstrators.

Also Alcatel recently announced to join the research program on wireless autonomous transducer solutions run by the Holst Centre. Alcatel will collaborate as a "Fellow Traveler" for a two-year period. With this partnership, Alcatel will be able to explore and evaluate potential market opportunities related to fixed access networks and residential multimedia applications based on research from the program on wireless sensor nodes.

The concept of Fellow Traveler partnerships is one of the collaboration opportunities within the wireless autonomous transducer solutions program, run by IMEC-Nederland at the Holst Centre. As such, the Holst Centre provides the partners with a platform where they can share market and technology trends, competitive analysis, standards and applications.

More info: www.holstcentre.com



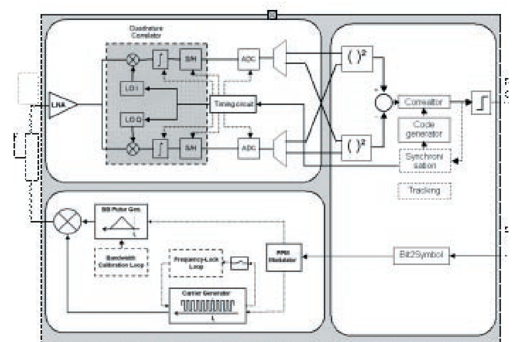
TECHNOLOGY REPORT

UWB Ultra-low-power radio building blocks evolve into a **full transceiver system**

IMEC developed a low-power digital baseband ultra-wideband (UWB) signal-processing core. Together with its previously realized UWB ultra-low-power transmitter and receiver, it completes the UWB low-power transceiver system for sensor networks.

Ultra-low-power radios combined with advanced energy-scavenging techniques enable a wide range of applications in sensor networks. IMEC has built an alternative for today's widely used Zigbee radios. The solution is based on ultra-wideband impulse Radio. This new technique for low-power radios has the potential to better serve sensor-network applications because of its ability to generate a wide range of data rates. When combined with intelligent circuit design, it is possible to make an ultra-low-power transmitter. The core of the transmitter is a pulse generator using a gating circuit that activates a ring oscillator when a pulse must be transmitted, avoiding useless power consumption between the pulses. A measured 0.18 full CMOS version shows a power consumption of 2mW while sending pulses at 30MHz repetition frequency. The transmitted pulses can be flexibly combined towards bits in function of the channel conditions. Average channel conditions, as e.g. along the front side of the human body, lead to a maximum data rate of 1Mbps using 30 pulses per bit. This solution clearly outperforms a typical Zigbee transmitter, achieving 250kbps at 18mW. On top of that, it shows an almost linear decrease in power consumption when lower data rates are required.

Recently, an analog receiver architecture was presented that is able to receive the UWB pulses. Now IMEC has completed the system with a low-power digital baseband UWB signal-processing core. It supports binary phase-shift keying (BPSK) and pulse-position modulation (PPM) modulations as well as the UWB preamble signals being defined in the IEEE 802.14a WPAN task group. Joint development of signal-processing algorithms and architectures along with on-chip data transfer, control, and partitioning leads to a low-power, yet flexible and scalable implementation. Simulation results validate the implemented algorithm on fading channels. The use of word-serial signal processing enables the system to be clocked at the pulse repetition frequency. This guarantees a low power consumption of 6mW simulated on top of the 30mW of the analog part using 30MHz pulse repetition frequency and designed in 0.18µm CMOS.



IMEC's UWB-IR transceiver system.

New patents

Europe

- Method of removing particles and a liquid from a surface of substrate. (EP 0 905 748)
- Apparatus for receiving GPS Glonass signals. (EP 0 924 532)
- Method of programming a flash EEPROM memory cell array optimized for low power consumption. (EP 1 189 238)
- A 2D Fifo device and method for use in block based coding applications. (EP 1 296 288)
- Electrostatic discharge protection device. (EP 1 482 554)

India

- Method of preparing solar cells front contacts. (IN 193582)

Taiwan

- Method to make markers for double gate SOI processing. (TW 1248646)
- Method for reducing the contact resistance of the connection regions of a semiconductor device. (TW 1248651)
- Method for fabricating self-aligned source and drain contacts in a Double gate FET with controlled manufacturing of a thin Si or non-Si channel. (TW 1248681)
- Method for fabricating self-aligned source and drain contacts in a Double gate FET with controlled manufacturing of a thin Si or non-Si channel. (TW 1253142)

USA

- Concurrent timed digital system design method and environment. (US 6,952,825)
- A method and apparatus for channel estimation. (US 6,990,061)
- Apparatus and method for determining the microelectromechanical devices (MEMS) (US 6,998,851)
- Switchable capacitor and method of making the same. (US 7,002,439)
- A design apparatus and a method for generating an implementable description of a digital system. (US 7,006,960)
- Constant resolution and space variant sensor array. (US 7,009,645)
- A method and apparatus for defect detection. (US 7,016,028)
- Method for making thin film devices for solar cells or silicon-on-insulator (SOI) applications. (US7,022,585)
- Insulating Barrier, NVM Bandgap Design. (US 7,026,686)
- Device for electrostatic discharge protection. (US 7,030,461)
- Method of producing semiconductor devices using chemical mechanical polishing. (US 7,033,941)
- Method for selective integration of air gaps and devices obtained by said method. (US 7,037,851)
- Method for forming quantum-mechanical memory and computational devices and devices obtained thereof. (US 7,042,004)
- A fluorinated hard mask for micropatterning of polymers. (US 7,042,091)

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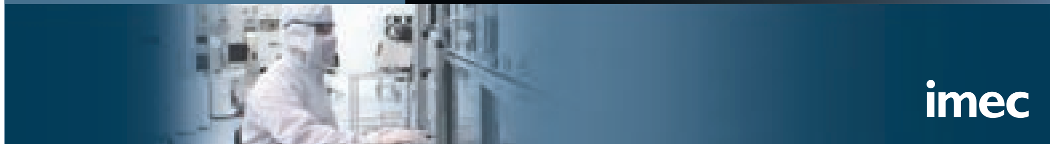
Event

THE IMEC RESEARCH-BUSINESS FORUM

Partnering for research: secure the future

Oct. 22-24, 2006 / Leuven / Belgium



ARRM06 will focus on the R&D challenges industry has to tackle to develop and manufacture future smart devices in a cost-efficient way and aims to bring industry executives and research managers together with senior IMEC research staff to discuss the technological challenges we are facing the coming years.

ARRM06 will feature no less than 14 sessions and 2 thematic forums with contributions from both IMEC and industry. Topics that will be covered will include a.o. advanced packaging and integration issues, beyond CMOS, technologies for seamless connectivity, emerging embedded platforms, organic devices and power electronics. This year's ARRM will also feature the International Wireless Sensor Network Forum that will highlight the challenges and trends of enabling technologies for the realization of intelligent sensor sensor networks both from a sensor platform and network infrastructure perspective.

For the first time, the ARRM06 will be followed by a European high-tech venture forum on Oct 25. In this one-day event, a selection of European startups will present their activities and plans for the future to senior industry and financial executives.

More info: www.arrm.be